Chapter 5.15

(1) If the processor issues a request that hits in the cache then the cache should be able to satisfy the request since it is otherwise idle when the write buffer is writting back to memory. If the cache is not able to satisfy hits while writing back from the write buffer, the cache will perform little or no better than the cache without the write buffer, since requests will still be serialized behind write backs.

(2) If the processor issues a request that misses in the cache then the cache will have to wait until the write back is complete since the memory channel is occupied. Once the memory channel is free, the cache is able to issue the read request to satisfy the miss