chapter 7.12

(1)

step 1

Assume we have two threads X and Y to run on these CPU that include the following operations

Thread X	Thread Y
A1 – takes 2 cycles to execute	B1 – no dependencies
A2 – depends on the result of A1	B2 – conflicts for a functional unit with B1
A3 – conflicts for a functional unit with A2	B3 – no dependencies
A4 – depends on the result of A2	B4 – depends on the result of B2

step 2

Depending on above assumptions the instructions flow is shown given below:

		0	1	2	3
Core 1	FU1	A1	A1		
	FU2	A3		A2	A4
Core 2	FU1	B1	B2	B4	
	FU2	B3			

Total 4 cycles take to execute these two threads

Total 7 issue slots are wasted due to hazards

(3) from 7.12

step 1

Assuming B1, B2, A2 and A3 all use the same functional unit. The SMT processor can schedule the operations as following:

	0	1	2	3	4	5
1	A1			B1	B2	B4
2	A3	B3	A2	A4		

Requires 6 cycles to execute, waste 4 issue slots.

step 2

Assuming B1, A2 use different functional units, the SMT processor can schedule the operations as following:

	0	1	2	3
1	A1	B1	B2	B4
2	A3	B3	A2	A4

Requires 4 cycles to execute, waste 0 issue slots