Chapter 7.7

(2) You have to serialize all the memory accesses among the processors and implement cache coherency protocol to guarentee only the most recently written value is returned. We could set synchronization instructions after each operation so that all cores see the same value on all nodes.

Chapter 7.8

(1) Consider we have P CPU's spread across T nodes in the CC-NUMA system, with each CPU having C memory blocks, and we maintain a byte of coherency information in each cache block. Then the amount of memory that will be present in the caches in a single node of the system to maintain coherency expressed as given below.

Equation

1 byte x C entries = number of bytes consumed in the cache for maintaining coherence.

(2) The amount of memory that will be present in each directory expressed as:

P bytes/entry x S/T = number of bytes needed to store coherency information in each directory on a single node